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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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VEDDER, PRICE, KAUFMAN & KAMMHOLZ
Christopher J. Reckamp
222 NORTH LaSALLE STREET
CHICAGO, IL 60601

EXAMINER	
LAY, MICHELLE K	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/244,270	YUE ET AL.	
	Examiner	Art Unit	
	Michelle K. Lay	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 14-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 14-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on 09/23/2005, has been entered and made of record. Claims 1, 2, and 14-42 are pending.

Response to Amendment/Argument

In Recent Applicant's Remarks, Applicant argued that the cited reference does not disclose "generating coordinate data representing an initial rasterization starting point estimate that is within the current tile" of recited claims, because the cited references (Duluk and Lentz) describe starting the rasterization of a triangle at a point outside of the triangle rather than an initial rasterization starting point estimate within the current tile. Examiner respectfully disagrees. Duluk teaches accepting or rejecting the sorted vertices with respect to the specific tile (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64). Thusly, although Duluk does not specifically disclose "generating coordinate data representing an initial rasterization starting point estimate that is within the current tile when one of the sorted vertex data lies within the current tile", such step ['generating coordinate data for rasterization starting point if the primitive is trivially accepted'] is necessarily required for displaying clipped image in rasterization process. In other word, starting/ending points have to be given or generated, in order to raster any type of polygon/primitives [**i.e. the method/function of generating rasterization starting point coordinates are not presented**]. Furthermore, since the system of

Duluk handles each tile on an individual basis, and also discards the data not within the current tile, these starting points would inherently be within the current tile.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim **23** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 23 recites the limitation "discard circuit" in line 1. Independent claim 14 fails to disclose a “discard” circuit as mentioned in claim 23. It is unclear if the circuit claimed in claim 14 is the “discard” circuit as claimed in claim 23. There is insufficient antecedent basis for this limitation in the claim.

Allowable Subject Matter

Claim **23** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-2,14-22** and **24-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk et al. (6,597,363) in view of Lentz et al. (5,446,836).

Regarding claim **1**, Duluk discloses that the claimed feature of a method comprising (See Fig 24, Fig 31, Fig 47-51: receiving vertex data corresponding to the vertices of a primitive, the vertex data including x-coordinate and y-coordinate position information (See col 44 line 46-49); sorting the vertex data in coordinate dependent fashion [i.e. "VtxYmin, VtxYmax, ...by **sorting the triangle vertices by their y coordinates**", "VtxXmin, VtxXmax...by **sorting the triangle vertices by their x coordinates**", whereas these sorted vertex are used to determine trivially accepted or rejected with respect to tile] (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64); generating region bits [i.e. "outcodes", "numerical numbers (3,1,9,2,8,6,4,12) on divided regions" in Fig 50] representing the location of the sorted vertex data ["sorted vertex"] with respect to a current tile [i.e. 8082 in Fig 50] being rendered [i.e. "outcodes", which generated and used to indicate ***reject primitives that are outside*** ['location of sorted vertex data' in recited claim] ***the view volume*** ['current tile' in recited claim]] (See Fig 50, col 54 line 1-6, col 54 line 14, col 81 line 8-33); generating coordinate data representing an initial rasterization starting point estimate [i.e. "the clipped line start points is generated...a new line start-point ...is generated..."; See col 76 line 30-36, Fig 45] when the region bits indicate that at least one of the sorted vertex data lies within the current tile being rendered [i.e. "trivially accepted primitives", primitives with its edge

intersecting a clip plane] and discarding the sorted vertex data of primitives that lie outside the boundary of the current tile being rendered [i.e. "trivially rejected primitives", which are outside the view volume] (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 115 line 53+); and providing the initial rasterization starting point estimate to a rasterizer. (See col 76 line 54-col 77 line 15, col 80 lines 25-48)

Duluk does not specifically disclose "generating coordinate data representing an initial rasterization starting point estimate that is within the current tile when one of the sorted vertex data lies within the current tile". However, such step ['generating coordinate data for rasterization starting point if the primitive is trivially accepted'] is necessarily required for displaying clipped image in rasterization process. In other word, starting/ending points have to be given or generated, in order to raster any type of polygon/primitives. Therefore, the raster operation of Duluk inherently meets the limitation in recited claim, as broadly claimed by applicant. [**i.e. the method/function of generating rasterization starting point coordinates are not presented**]. Additionally, since the system of Duluk handles each tile on an individual basis, these starting points would inherently be within the current tile. As to the teaching of Lentz (See "starting points" in Fig 4A and B, where "starting point" in Fig 4B is smarter algorithm of rasterization; See col 3 line 39-45), it would have been obvious to one skilled in the art to incorporate teaching of Lentz (See "starting point" in Fig 4A, Fig 4B, Fig 5, Fig 6, Fig 9, col 3 line 36-col 4 line 46) into the teaching of Duluk, in order to decrease a substantial time of the rasterization efficiently and to minimize computation time for rasterization (by eliminating the image process on invisible side) [i.e. See "In

order to reduce the unnecessary processing ...the clipped line start points is generated...a new line start-point ...is generated..." col 76 line 25-36, Fig 45 of Duluk; Also see "smarter algorithm", "efficient" in col 3 line 39-45 of Lentz], as such improvement [finding starting point for rasterization] is also advantageously desirable in the teaching of Duluk for rendering the image at faster time by reducing the unnecessary processing of portion of clipped or invisible primitive.

Regarding claim **2**, Duluk disclose that generating an orientation bit representing an orientation of a line connecting the first and second vertices of the sorted primitive with respect to a line connecting the first and third vertices of the sorted primitive before generating the initial rasterization starting point coordinates. (See col 34 lines 1-2, col 77 lines 26-37) Furthermore, using orientation of triangles to classify or organize the triangle variable or/and calculating an orientation of two side of a triangle is necessarily required for classifying the triangle base on its shape [i.e. right oriented triangle, left oriented triangle], as suggested in the teaching of Lentz (See col 7 line 43-47, col 8 line 24-32), in order to render/raster the triangle/primitives effectively with easy manner.

Regarding claim **14**, claim 14 is similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claim 14.

Regarding claim **15**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that the initial rasterization starting point estimation circuit includes a trivial

accept circuit operative to provide the initial rasterization starting point in response to the region bits. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 115 line 53+)

Regarding claim **16**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that the vertex data is sorted in y-coordinate fashion and the trivial accept circuit provides the x-coordinate and sorted y-coordinate rasterization starting point of a non-discarded primitive. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **17**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the vertex data. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim **18**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that the boundary interception point generated by the intercept calculation circuit represents the initial rasterization point starting point coordinate. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim **19**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the sorted

vertex data. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim **20**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that the trivial accept circuit comprises a logic gate coupled to a corresponding subset of the region bits. (See col 125 line 16-col 126 line 33)

Regarding claim **21**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that the logic gate is an AND gate. (See col 125 line 16-col 126 line 33)

Regarding claim **22**, Duluk discloses that the region bits define the top edge, bottom edge, right edge and left edge of a current tile being rendered. (See Fig 50)

Regarding claim **24**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that the x-coordinate and y-coordinate of the initial rasterization starting point to the boundary intercept points. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim **25**, claim 25 is similar in scope to the claim 2, and thus the rejection to claim 2 hereinabove is also applicable to claim 25.

Regarding claim **26**, refer to the discussion for the claim 1 hereinabove, Duluk discloses that determining the relative positioning between the vertices of the primitive. (See col 34 line 11-13, col 34 line 34-36, col 44 line 46-64)

Regarding claims **27-28**, claims 27-28 are similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claims 27-28.

Regarding claim **29**, Duluk discloses that the position data includes x coordinate and y coordinate position data, and the sorting step comprises arranging the position data in y coordinate order. [i.e. "VtxYmin, VtxYmax, ...by sorting the triangle vertices by their y coordinates"](See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **30**, Duluk discloses that the primitive are arranged in descending y coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **31**, Duluk discloses that the primitives are arrange in ascending y-coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **32**, Duluk discloses that the position data includes x coordinate and y coordinate position data, and the sorting step comprises arranging the position

data in x coordinate order. [i.e. "VtxXmin, VtxXmax...by sorting the triangle vertices by their x coordinates] (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **33**, Duluk discloses that the primitive are arranged in descending x coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **34**, Duluk discloses that the primitives are arrange in ascending x-coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim **35**, Duluk discloses that comparing the x coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the x coordinate position is greater than the largest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim **36**, Duluk discloses that comparing the x coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the x coordinate position is less than the smallest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim **37**, Duluk discloses that comparing the y coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the y coordinate position is greater than the largest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim **38**, Duluk discloses that comparing the y coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the y coordinate position is less than the smallest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim **39**, Duluk discloses that generating an initial x coordinate and an initial y coordinate based on the corresponding x coordinate and sorted y coordinate of the primitive within the current tile. (See col 76 line 25-36, Fig 45, Also See "starting points" in Fig 4A and B, where "starting point" in Fig 4B is smarter algorithm of rasterization; col 3 line 39-45 in Lentz)

Regarding claim **40**, Duluk discloses that generating the initial x coordinate and y coordinate based on the boundary region of the current tile. (See col 76 line 25-36, Fig 45, Also See col 3 line 39-45 in Lentz)

Regarding claim **41**, claim 28 is similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claim 28.

Regarding claim **42**, claim 42 is similar in scope to the claim 39, and thus the rejection to claim 39 hereinabove is also applicable to claim 42.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle K. Lay whose telephone number is (571) 272-7661. The examiner can normally be reached on Monday-Thursday from 7:30am to 5:00pm. The examiner can also be reached on alternate Fridays from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi, can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michelle K. Lay
Patent Examiner
Art Unit 2672

12.19.2005 mkl

RICHARD HJERPE 12/21/05
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600